

FIG. 1

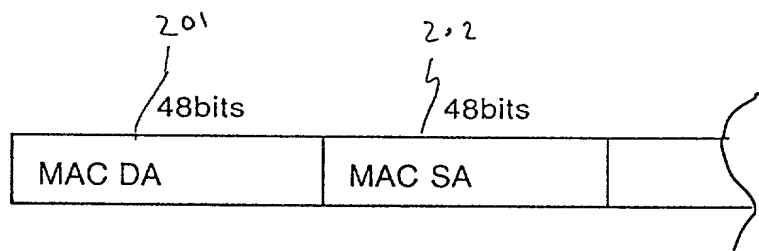


FIG. 2

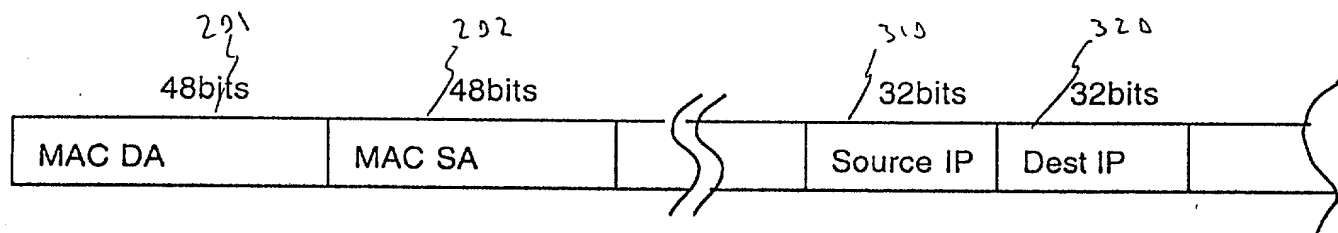


FIG. 3

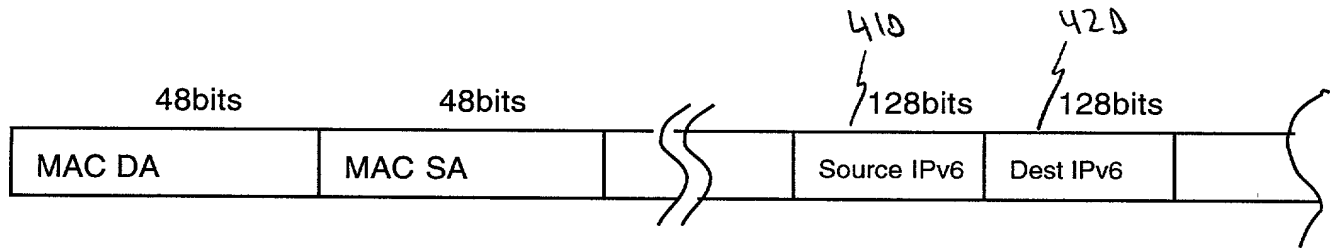


FIG. 4

500

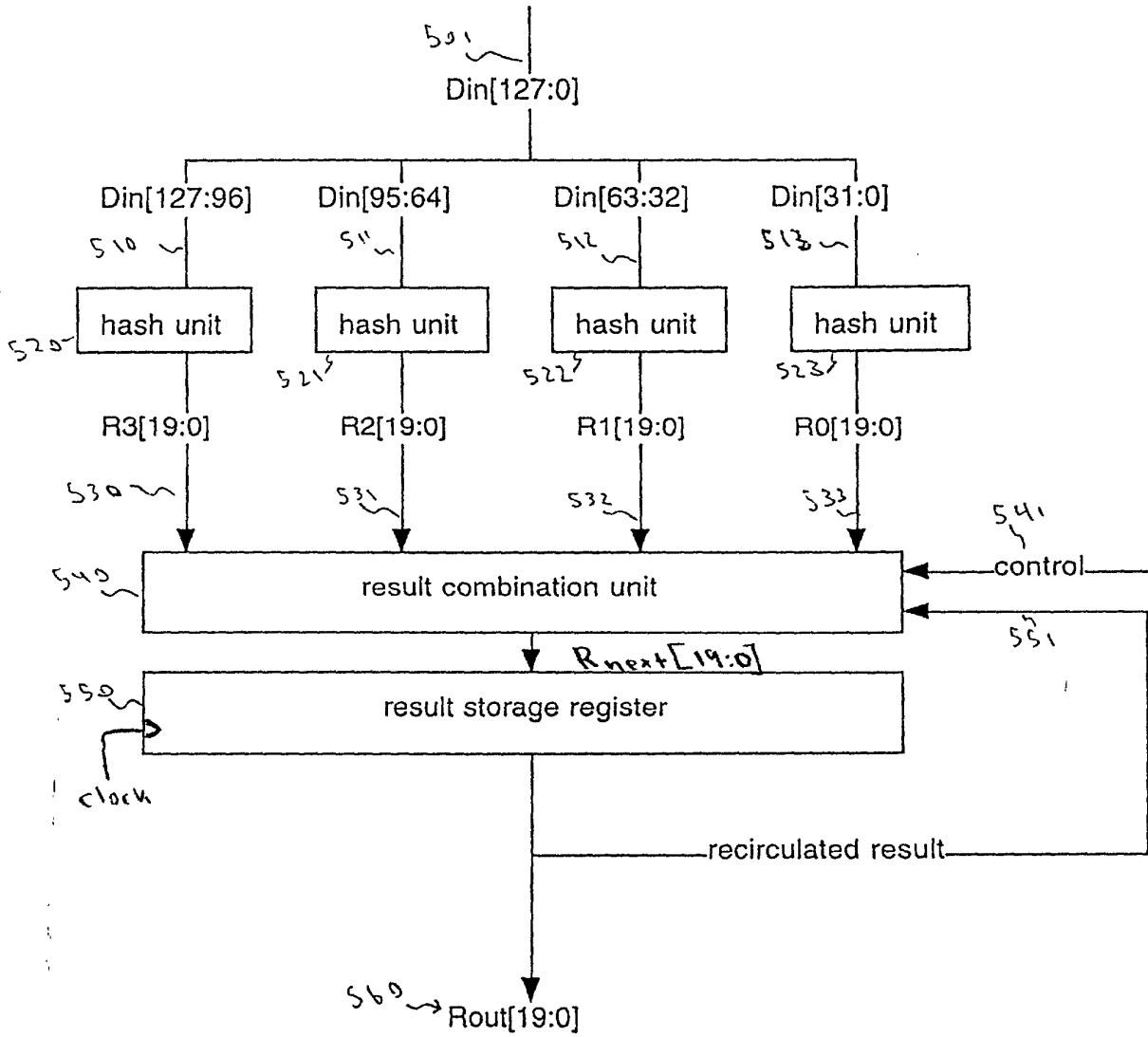


FIG. 5

```
if (control == 0)
{
  Rnext = R3 XOR R2 XOR R1 XOR R0;
}
else
{
  Rnext = R3 XOR R2 XOR R1 XOR R0 XOR Rout;
}

Rout <= Rnext on each positive clock edge
```

FIG. 6

700

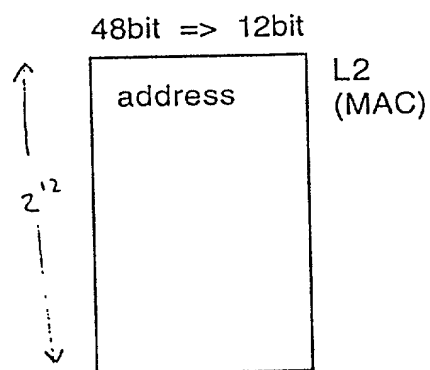


FIG. 7

800

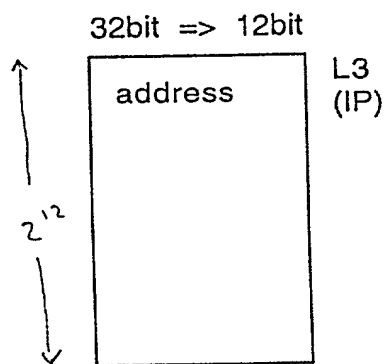


FIG. 8

903

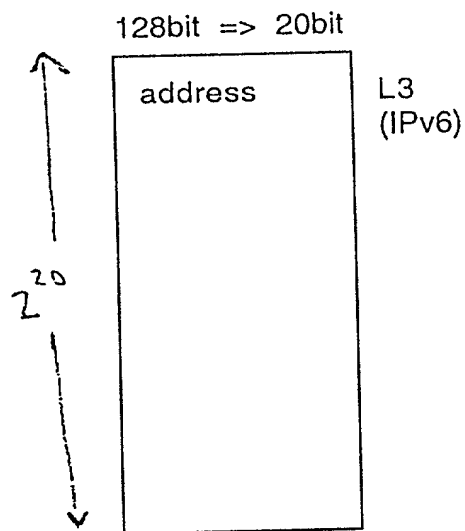


FIG. 9

1000

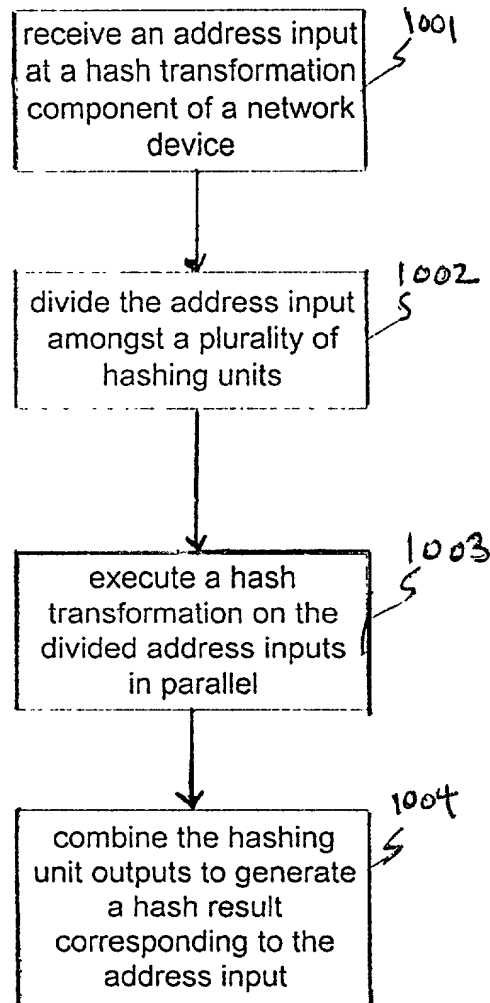


FIG. 10